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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,564	LLOYD, STACEY G.	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 and 7-19 have been examined.

2. Acknowledgement of papers filed: amendment on 3/13/06. The papers filed have been placed on record.

Withdrawn Objections and Rejections

3. Applicant, via amendment, has overcome the objections to claims 16 and 17 set forth in the previous Office Action. Consequently, these objections have been withdrawn by the Examiner.

4. Applicant, via amendment, has overcome the 35 U.S.C. 112 rejections to claims 8-10 set forth in the previous Office Action. Consequently, these rejections have been withdrawn by the Examiner.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1-5, 8-9, 11-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al, U.S. Patent 5,796,972, herein referred to as Johnson, in view of Handy, Jim, The Cache Memory Book, 2nd ed., herein referred to as Handy.

7. As per claim 1, Johnson teaches a method for handling operations within a hardware device, comprising:

a. Providing within the device information regarding an operation, the operation having a predetermined responsive output as encoded within a transaction lookup table (Fig. 8, Ucode ROM 294) and an alternative responsive output stored in a register (Fig. 8, Patch RAM 296), the provided information including information identifying the operation: [(The predecode block 290 provides identifying information for each operation. Col. 11, line 62 to col. 12, line 18. The ROM 294 is given an address and outputs the predetermined operation to a multiplexer 298. The Ram 296 contains alternative operations, and supplies them to the multiplexer 298.]

b. Selecting at least some of the identifying information of the operation to output to the transaction lookup table, and output of the transaction lookup table are input into a multiplexer: [Figs. 8 & 10, the identifying information is provided to the Ucode ROM 294 via line 358 and the output of the Ucode ROM 294 is output to the multiplexer 298.]

c. Selecting the alternative responsive output for the operation instead of the predetermined responsive output based upon the identifying information and directing the multiplexer to output the alternative responsive output, such that the multiplexer effectively converts at least some of the information regarding the operation based upon the selected identifying information: [Based on the identifying information, the ID RAM produces a CS RAM SEL bit on line 362

which indicates which output to choose, the ROM or RAM (lookup table or alternative register). See figs. 8 and 10, col. 11, line 62 to col. 12, line 33 and co. 13, line 3-17.]

d. And executing the operation based upon the converted information: [The instructions are forwarded on the output of the multiplexer to execution units. (Figures 4 and 8)]

8. Johnson teaches the ID RAM as a index-able memory, wherein the pre-decode unit 290 provides an indexing address, and the ID RAM further converts this into another address for the ROM or RAM and also provides an associated CS RAM SEL bit. Therefore, Johnson fails to teach a comparator, wherein the output of the comparator provides an input to the multiplexer.

9. However, Handy teaches that CAM memories are well known in the art and are a different method of lookup table memories. Instead of providing an address as an input, a data input is provided, which is then compared against a stored value. When a match is present, the corresponding stored data is output. Implementing the ID RAM as a CAM memory instead of an indexed memory would cause the identifying information to be provided to a comparator and some of the decoded identifying information would still be provided to the UCODE ROM 294. The output of the comparator (The CAM memory as a whole performs comparisons, and therefore is a comparator) would consist of a CS RAM SEL bit, which results from a match and is input to the multiplexer to select from which memory, the predetermined (ROM 294) or the alternative (RAM 296), the output is to be selected from. (Handy, pages 14-18)

10. It would have been obvious to one of ordinary skill in the art to replace the index-able memory of Johnson with the CAM memory of Handy since CAM memories are widely known in the art as alternatives to index-able memories and allows any entry to point to any location and have parallel access to each comparator so there is no hindrance on performance. Furthermore, a CAM memory would logically perform the same operation the index-able memory is performing. An identifying data portion is input to the memory, and the associated data is retrieved, in both the index-able memory and the CAM memory.

11. As per claim 2, Johnson, in view of Handy, teaches the method of claim 1, wherein the provided information is within a register of the device: [The predecode block 290 provides information for each operation. Col. 11, line 62 to col. 12, line 18. It comes from an entry in the memory unit (instruction memory 252), which is a register within the device.]

12. Furthermore, although Johnson, in view of Handy, does not specifically teach pipeline latches, Examiner takes Official Notice that pipeline latches (registers) between stages in a processor are very well known and allow proper timing between combinational logic stages, such as the fetching, predecoding, decoding, execution, etc. Specifically teaching pipeline registers would cause there to be a register between the different stages of the pipeline, including between the memory and decode stages, and thus, the provided information would be within a register of the device.

13. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include pipeline latches (registers) between stages since

Examiner takes Official Notice that pipeline latches allow proper timing between stages in a pipelined processor and are well known in the art.

14. As per claim 3, Johnson, in view of Handy, teaches the method of claim 1, wherein the identifying information is within a register of the device: [The predecode block 290 provides identifying information for each operation. Col. 11, line 62 to col. 12, line 18. It comes from an entry in the memory unit (instruction memory 252), which is a register within the device.]

15. Furthermore, although Johnson, in view of Handy, does not specifically teach pipeline latches, Examiner takes Official Notice that pipeline latches (registers) between stages in a processor are very well known and allow proper timing between combinational logic stages, such as the fetching, predecoding, decoding, execution, etc. Specifically teaching pipeline registers would cause there to be a register between the different stages of the pipeline, including between memory and decode stages, and thus, the provided information would be within a register of the device.

16. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include pipeline latches (registers) between stages since Examiner takes Official Notice that pipeline latches allow proper timing between stages in a pipelined processor and are well known in the art.

17. As per claim 4, Johnson, in view of Handy, teaches the method of claim 1, wherein the converted information is within a register of the device: [The converted information is stored in an entry in the RAM 296. An entry in the RAM 296 is a register in the device. Figs. 8 & 10, col. 11, line 62 to col. 12, line 33.]

18. As per claim 5, Johnson, in view of Handy, teaches the method of claim 1, wherein the step of providing information regarding the operation comprises providing the predetermined responsive output and the alternative responsive output: [The RAM 296 outputs the alternative responsive output and the ROM 294 outputs the predetermined responsive output. Figs. 8 & 10, col. 11, line 62 to col. 12, line 33.]

19. As per claim 8, Johnson teaches a method for redirecting transactions [instructions] within a hardware device, wherein transactions occurring within said device contain fields of information regarding the transaction [inherently, the instructions contain fields of information], the method comprising the steps of:

e. Loading all of said fields necessary to identify a transaction into a first register: [The entries within Instruction Memory 252 contain instructions (inherently loaded), and since they can be decoded and executed, the instructions inherently include all of the fields necessary to identify the instructions. Fig. 7, col. 1, line 62 to col. 12, line 18.]

f. Selecting which fields of said first register are to be acted upon and inputting the selected fields into a multiplexer: [Johnson teaches using the opcode as an index into the ID RAM. Therefore there is a selection of the index field of an instruction from the first register (an entry in memory).]

g. Converting the transaction information to be redirected through a pre-programmed value for each said field by inputting into the multiplexer a predetermined responsive value into the multiplexer, the predetermined responsive value stored in a transaction lookup table and an alternative

responsive output stored in a register, the multiplexer also receiving input such that the multiplexer outputs the alternative responsive value for the transaction based upon the ID RAM's selecting output, CS RAM SEL. Fig. 8, 10, col. 11, line 62 to col. 12, line 33.]

20. Johnson teaches the ID RAM as a index-able memory, wherein the pre-decode unit 290 provides an indexing address, and the ID RAM further converts this into another address for the ROM or RAM and also provides an associated CS RAM SEL bit. Therefore, Johnson fails to teach the multiplexer also receiving input from *a comparator*, such that the multiplexer outputs the alternative responsive value for the transaction based upon *the comparator comparing the selected fields to the transaction resulting in a match.* Johnson further fails to teach the output from the multiplexer (Examiner's interpretation of "said new transaction results") is sent to a register.

21. However, Handy teaches that CAM memories are well known in the art and are a different method of lookup table memories. Instead of providing an address as an input, a data input is provided, which is then compared against a stored value. When a match is present, the corresponding stored data is output. Implementing the ID RAM as a CAM memory instead of an indexed memory would cause the identifying information to be provided to a comparator and some of the decoded identifying information would still be provided to the UCODE ROM 294. The output of the comparator (The CAM memory as a whole performs comparisons, and therefore is a comparator) would consist of a CS RAM SEL bit, which results from a match and is input to the multiplexer to select from

which memory, the predetermined (ROM 294) or the alternative (RAM 296), the output is to be selected from. (Handy, pages 14-18)

22. It would have been obvious to one of ordinary skill in the art to replace the index-able memory of Johnson with the CAM memory of Handy since CAM memories are widely known in the art as alternatives to index-able memories and allows any entry to point to any location and have parallel access to each comparator so there is no hindrance on performance. Furthermore, a CAM memory would logically perform the same operation the index-able memory is performing. An identifying data portion is input to the memory, and the associated data is retrieved, in both the index-able memory and the CAM memory.

23. Furthermore, although Johnson, in view of Handy, does not specifically teach pipeline latches, Examiner takes Official Notice that pipeline latches (registers) between stages in a processor are very well known and allow proper timing between combinational logic stages, such as the fetching, predecoding, decoding, execution, etc. Specifically teaching pipeline registers would cause there to be a register between the different stages of the pipeline, including between the decode stages and the execution, and thus, the outputted results from the multiplexer 298 would be sent to a register.

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include pipeline latches (registers) between stages since Examiner takes Official Notice that pipeline latches allow proper timing between stages in a pipelined processor and are well known in the art.

25. As per claim 9, Johnson, in view of Handy, teaches the method of claim 8, wherein the step of loading said field necessary to identify a transaction includes first loading transaction identifications. [The entries within Instruction Memory 252 contain instructions (inherently loaded), and since they can be decoded and executed, the instructions inherently include all of the fields necessary to identify the instructions. Fig. 7, col. 1, line 62 to col. 12, line 18. See also the Rejection to claim 8 and the 35 U.S.C. 112 Rejection to claim 9 above.]

26. As per claim 11, given the similarities between claim 1 and claim 11, the arguments as stated for the rejection of claim 1 also apply to claim 11.

27. As per claim 12, Johnson, in view of Handy, teaches the method of claim 11, wherein the step of creating a list of identified operations includes first loading transaction identification: [The list of identified operations is stored in the ID RAM (Fig. 8, 10 of Johnson), which, in view of Handy, is a CAM memory (see Handy, pages 14-18). The CAM memory ID RAM is inherently loaded with the list, or the CAM memory ID RAM would not contain any data.]

28. As per claim 14, given the similarities between claim 1 and claim 14, the arguments as stated for the rejection of claim 1 also apply to claim 14.

29. As per claim 15, Johnson, in view of Handy, teaches the system of claim 14, wherein one or more of said storage means may be selectively enable or disabled: [From one point of view, the MUX effectively causes an enabling or disabling of the Ucode ROM 294 and Patch RAM 296. From another point of view, the address that indexes into the RAM 296 and ROM 294 causes an enabling of an entry of the RAM

296 and ROM 294 and a disabling of the rest of the entries in the RAM 296 and ROM 294. Fig. 8, col. 11, line 62 to col. 12, line 33.]

30. As per claim 16, Johnson teaches in a data processing system utilizing a hardware control device in which a given operation results in a predetermined response for that operation, a system for providing a programmable redefinition of allowed instructions and associated responses within said hardware device including:

h. First register means which contains fields to identify preselected operations which may occur within the system: [The Instruction Memory contains instruction in entries (registers) and contains identifying information which is decoded to indicate operations. Fig. 8]

i. Second register means which operates upon selected fields in the first register means to further define a criteria for which redirecting a response is desired: [ID RAM 352 contains multiple registers. They operate on the first register means' selected field that is input (figs. 8 & 10) by interpreting it and outputting further defined criteria for redirecting a response. Col. 11, line 62 to col. 12, line 33.]

j. Transaction lookup table means to output a standard value for the current operation: [Ucode Rom 294 contains the standard values. Figs. 8 & 10, col. 11, line 62 to col. 12, line 33.]

k. And multiplexer means receiving input indicating the desired selection (via line 302), transaction lookup table means (via line 293) and outputting a substitute value for a predetermined value the current operation [when the CS

RAM SEL bit selects the Patch RAM 296, the substitute value replaces the predetermined value], the substitute value stored in a register (Patch RAM 296) and the predetermined value stored in a transaction lookup table (Ucode ROM 294): [Figs. 8 & 10, col. 11, line 62 to col. 12, line 33.]

31. Johnson teaches the ID RAM as a index-able memory, wherein the pre-decode unit 290 provides an indexing address, and the ID RAM further converts this into another address for the ROM or RAM and also provides an associated CS RAM SEL bit. Therefore, Johnson fails to teach the multiplexer also receiving input from *a comparator* means that is used for selecting an input of the MUX for output.

32. However, Handy teaches that CAM memories are well known in the art and are a different method of lookup table memories. Instead of providing an address as an input, a data input is provided, which is then compared against a stored value. When a match is present, the corresponding stored data is output. Implementing the ID RAM as a CAM memory instead of an indexed memory would cause the identifying information to be provided to a comparator and some of the decoded identifying information would still be provided to the UCODE ROM 294. The output of the comparator (The CAM memory as a whole performs comparisons, and therefore is a comparator) would consist of a CS RAM SEL bit, which results from a match and is input to the multiplexer to select from which memory, the predetermined (ROM 294) or the alternative (RAM 296), the output is to be selected from. (Handy, pages 14-18)

33. It would have been obvious to one of ordinary skill in the art to replace the index-able memory of Johnson with the CAM memory of Handy since CAM memories are

widely known in the art as alternatives to index-able memories and allows any entry to point to any location and have parallel access to each comparator so there is no hindrance on performance. Furthermore, a CAM memory would logically perform the same operation the index-able memory is performing. An identifying data portion is input to the memory, and the associated data is retrieved, in both the index-able memory and the CAM memory.

34. As per claim 17, given the similarities between claim 15 and claim 17, the arguments as stated for the rejection of claim 15 also apply to claim 17.

35. As per claim 18, given the similarities between claim 1 and claim 18, the arguments as stated for the rejection of claim 1 also apply to claim 18.

36. Claims 7, 10 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al, U.S. Patent 5,796,972, herein referred to as Johnson, in view of Handy, Jim, The Cache Memory Book, 2nd ed., herein referred to as Handy, and further in view of "The PowerPC Architecture: A specification for a new family of RISC processors", hereinafter PowerPC.

37. As per claim 7, Johnson, in view of Handy, teaches the method of claim 5, however does not specifically state what makes up the operation identifications. Johnson, in view of Handy, teaches using a CAM memory in place of the ID RAM of Johnson (fig. 10, item 352), however, it is not specified what information identifies an operation since the instruction set is not defined

38. However, the PowerPC Architecture has taught operation identifications in instructions comprising fields for operation identification (OPCD field, PowerPC, page

21), length (L field, PowerPC, page 21), attribute field (RA field, PowerPC, page 22),and target (BF field, PowerPC, page 19) of each operation. One of ordinary skill in the art would have recognized that using the PowerPC Architecture as the architecture in the method/apparatus of Johnson, in view of Handy, would be beneficial given the expansive software base that is compatible with the PowerPC architecture. Using an architecture with such a wide acceptance in the field allows for the method/apparatus to run a wide variety of programs. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the PowerPC architecture in the method/apparatus of Johnson, in view of Handy, in order to provide an established instruction set with an expansive collection of compatible software programs.

39. As per claim 10, given the similarities between claim 7 and claim 10, the arguments as stated for the rejection of claim 7 also apply to claim 10.

40. As per claim 13, given the similarities between claim 7 and claim 13, the arguments as stated for the rejection of claim 7 also apply to claim 13.

41. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al, U.S. Patent 5,796,972, herein referred to as Johnson, in view of Handy, Jim, The Cache Memory Book, 2nd ed., herein referred to as Handy, and further in view of IBM Technical Disclosure Bulletin, Vol. 37, No. 03, hereinafter IBM.

42. As per claim 19, Johnson, in view of Handy, does not specifically teach wherein the comparator is responsive to a mask of the identifying information. Johnson is silent on the specific identifying information, and only teaches that a decoded instruction

address is provided (col. 11, line 62 to col. 12, line 9). Furthermore, Johnson, in view of Handy, teaches comparing identifying information of an instruction in a CAM style memory ID RAM, but again, there is no specific teaching as to what the identifying information is exactly made up of.

43. IBM teaches only sending the opcode as identifying information, and therefore masking the remaining portions of the instruction, when deciding whether or not an instruction needs to be substituted. (See figure in upper-right hand corner).

44. It would have been obvious to one of ordinary skill in the art to mask the identifying information of the instruction to select only the opcode to be send to the CAM memory, ID RAM, since an opcode's purpose is to identify instructions and since IBM explicitly teaches masking instruction information to produce only an opcode for identifying purposes.

Response to Arguments

45. Applicants arguments filed on 3/13/06 have been fully considered but they are not persuasive.

46. Applicant argues in substance that the novelty/rejection of claims 1-5, 8-9, 11-12 and 14-18.

"Handy is not properly combined with Johnson for two separate and independent reasons. First, there is no reason, suggestion, or motivation to modify Johnson as per Handy as recited by the Examiner. Second, Handy in fact teaches away from combination with Johnson."

"Examiner stated...

> It would have been obvious to one of ordinary skill in the art to replace the index-able memory of Johnson with the CAM memory of Handy since CAM memories are widely known in the art as alternatives to index-able memories and allows any entry to point to any location and have parallel access to each comparator so there is no hindrance on performance. Furthermore, a CAM memory would logically perform the same operation the index-able memory is performing. An identifying data portion is input to the memory,

> and the associated data is retrieved, in both the index-able memory and the CAM memory."

"Applicant believes that this stated suggestion or motivation [to] modify Johnson per Handy has two parts. The first part is that it would have been obvious to modify Johnson to employ the CAM memories of Handy because "CAM memories are widely known in the art as alternative to indexable memories." However, the MPEP is clear that the 'fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness.' (MPEP 2143.01 IV)"

"The second part of the Examiner's stated suggestion or motivation to modify Johnson per Handy is that "CAM memories... allow[] any entry to point to any location and have parallel access to each comparator so there is no hindrance on performance' and that 'a CAM memory would logically perform the same operation the indexable memory is performing.' Applicant submits that in substance the Examiner is saying here that you can use the CAM memories of Handy instead of the indexable memories of Johnson because: 1) they logically perform the same thing; and, 2) there is no hindrance on performance in doing so, since CAM memories allow any entry to point to any location and have parallel access. However, the MPEP is also clear that the 'fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness.' (MPEP 2143.01.III.)"

"Now, the Examiner is saying that CAM memories logically perform the same way as indexable memories, and that replacing the indexable memories of Johnson with the CAM memories of Handy results in no hindrance on performance. However, both of these things go to the fact that Johnson '*can* be combined with Handy" - and most significantly, neither 'suggests the desirability of the combination.' That is, that CAM memories logically perform like indexable memories does not suggest the desirability of using CAM memories instead of indexable memories (i.e., why they should be used) instead of indexable memories."

47. These arguments are not found persuasive for the following reasons:

I. To begin, Examiner agrees that the "first part" of the motivation provided was the fact that it was possible to replace the indexable memory with the CAM memory of Handy. This was merely used to establish that a CAM memory is a widely known alternative to indexable memories, and was not soley relied upon for the motivation, which coincides with MPEP 2143.01 IV, which states, the 'fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness.' (Emphasis added by Examiner). Tthe statement that CAM memories and indexable

memories are known alternatives compliment the additional benefits provided to establish motivation for the combination, and the statement was not relied upon by itself.

m. The "second part" of the motivation, as it has been categorized, is that CAM memories "allow[] any entry to point to any location and have parallel access to each comparator so there is no hindrance on performance." However, to clarify, there are two separate points within the "second part" of the motivation. The first is that any entry in a CAM can point to any location in the ROM and RAM. Handy states, "any main memory address can be mapped into any directory location," because of it's fully associative properties, the CAM memory is flexible and more efficient than a set associative or directly accessed memory. This is an advantage that would provide motivation to one of ordinary skill in the art to replace the indexable memory of Johnson with the CAM memory of Handy.

n. Furthermore, the second point within the "second part" states that CAM memories "have parallel access to each comparator so there is no hindrance on performance." The fact that there is parallel access to entries in a CAM causes faster access, and therefore there is an inherent advantage because the access time for a CAM is less. CAMs do not require serial access to each comparator entry, thus there is no hinderance on performance, and in fact, access time is sped up. This is evidenced by both Naji, U.S. Patent 6,304,477 (Col. 1, lines 25-38) and Eskandari-Gharnin et al., U.S. Patent 5,602,764 (Col. 1, lines 6-16). The

parallelized access, which causes speed up in access time, also provides motivation to one of ordinary skill in the art.

48. Applicant further argues in substance that the novelty/rejection of claims 1-5, 8-9, 11-12 and 14-18.

"Handy teaches away from combination with Johnson"
"There are two big disincentives and demotivations to modify Johnson in view of Handy. First, Handy's CAM memories are more complicated to use than other, simpler schemes (like Johnson's indexable memories), and these other, simpler schemes perform nearly as well. Therefore, because Johnson's cache memory scheme performs just fine the way it is recited, there is no motivation to modify it to instead use CAM memories, wherein doing so would be much more complicated than simply using indexable memories as recited in Johnson, with little performance benefit at best. For this reason alone, Handy teaches away from modification of Johnson per Handy."
"Indeed, Applicant submits that insofar as there are 'only two kinds of CAMS available on the market today,' attempting to use the CAM memories of HANDY as a replacement for the indexable memories of Johnson would require a substantial reconstruction and redesign of the scheme taught in Johnson. That is, where Handy admits in substance that CAM memories are much more complex – insofar as Handy states that other types of memories are much simpler than CAM memories – and where there are only two kinds of CAMs available on the market today, Applicant submits that the Examiner cannot presume that the indexable memories of Johnson could be easily substituted by those of ordinary skill within the art by the CAM memories of Handy... Indeed, since there are only two kinds of CAMs available on the market today, Johnson's cache memory scheme performs just fine the way it is recited, there is no motivation to modify it to instead use CAM memories, where doing so would be more expensive, as admitted by Handy and which is also supported by the fact that there are only two kinds of CAMs available on the market today, and where little performance benefit at best would result. For this reason alone as well, Handy teaches away from modification of Johnson per Handy."

49. These arguments are not found persuasive for the following reasons:

o. First, Examiner notes that a specific advantage is taught by Handy, that is, "if the cache directory is a CAM, then *any* main memory address can be mapped into *any* directory location." Hence, the CAM memory is flexible. Furthermore, as the CAM has parallel comparisons, access to the CAM have increased speed

(for further evidence, see col. 1, lines 6-16 of Eskandari-Charnin, U.S. Patent 5,602,764, and Col. 1, lines 25-38 of Naji, U.S. Patent 6,304,477.)

p. Second, Examiner concedes that Handy teaches disadvantages of using a CAM memory as a cache, however, as with most design options in computer architecture, different implementations have different advantages as well as disadvantages. As this is a text book, dealing specifically with cache memory in the typical memory hierarchy system, the listed disadvantages do not inherently apply to the memory needed in Johnson, and furthermore, the book was published in 1998, thus some of the disadvantages of CAMs have been addressed. For instance, the indexable memory in fig. 9 only contains 10 entries, which is considerably smaller than a typical low level cache. Thus, the expense and complexity described in Handy would no longer be a significant factor and would not deter one of ordinary skill in the art from combining the references.

q. Furthermore, while Examiner believes the Handy reference alone supports the 35 U.S.C. 103 rejection, further support can be found in col. 1, lines 6-16 of Eskandari-Charnin, U.S. Patent 5,602,764, explicitly teaches support for the assertion that CAMs are used to speed up access to memories. Additional support is taught in Col. 1, lines 25-38 of Naji, U.S. Patent 6,304,477, wherein it is stated, "The time to access information in a memory can be reduced drastically if the stored data can be identified by the content rather than by an address. CAMs or associated memories are used *extensively in cache memories and translation look-aside buffers*." (Emphasis added by Examiner) The Naji

reference was printed in 2001, three years later than the updated Handy reference, thus this supports the assertion that CAM disadvantages have been addressed and are now commonly used memory types (even being used for cache memories) and have the explicitly stated speed benefit as well.

Conclusion

50. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR

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